University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #2 – Solution
August 5, 2009

Name ________________________________

Perm # ________________________________

Lab Section ____________________________

Problem #1 (35 points) ___________

Problem #2 (35 points) ___________

Problem #3 (30 points) ___________

Total (100 points) ___________

- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions on the exam.

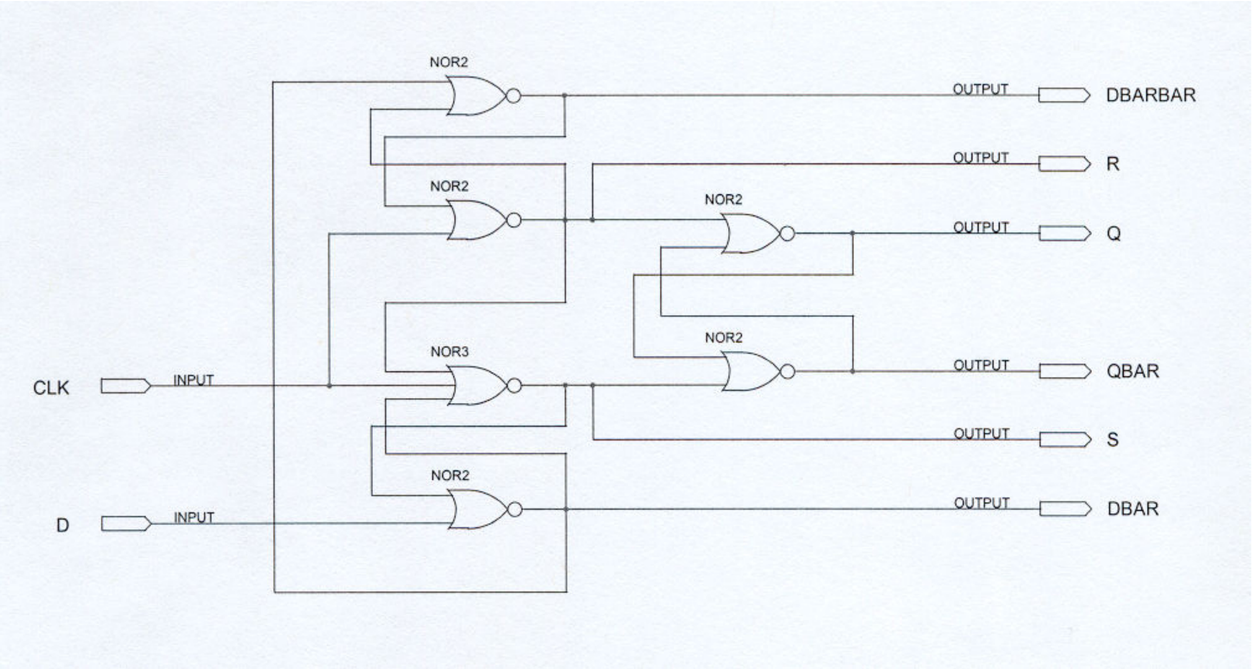
Problem #1.

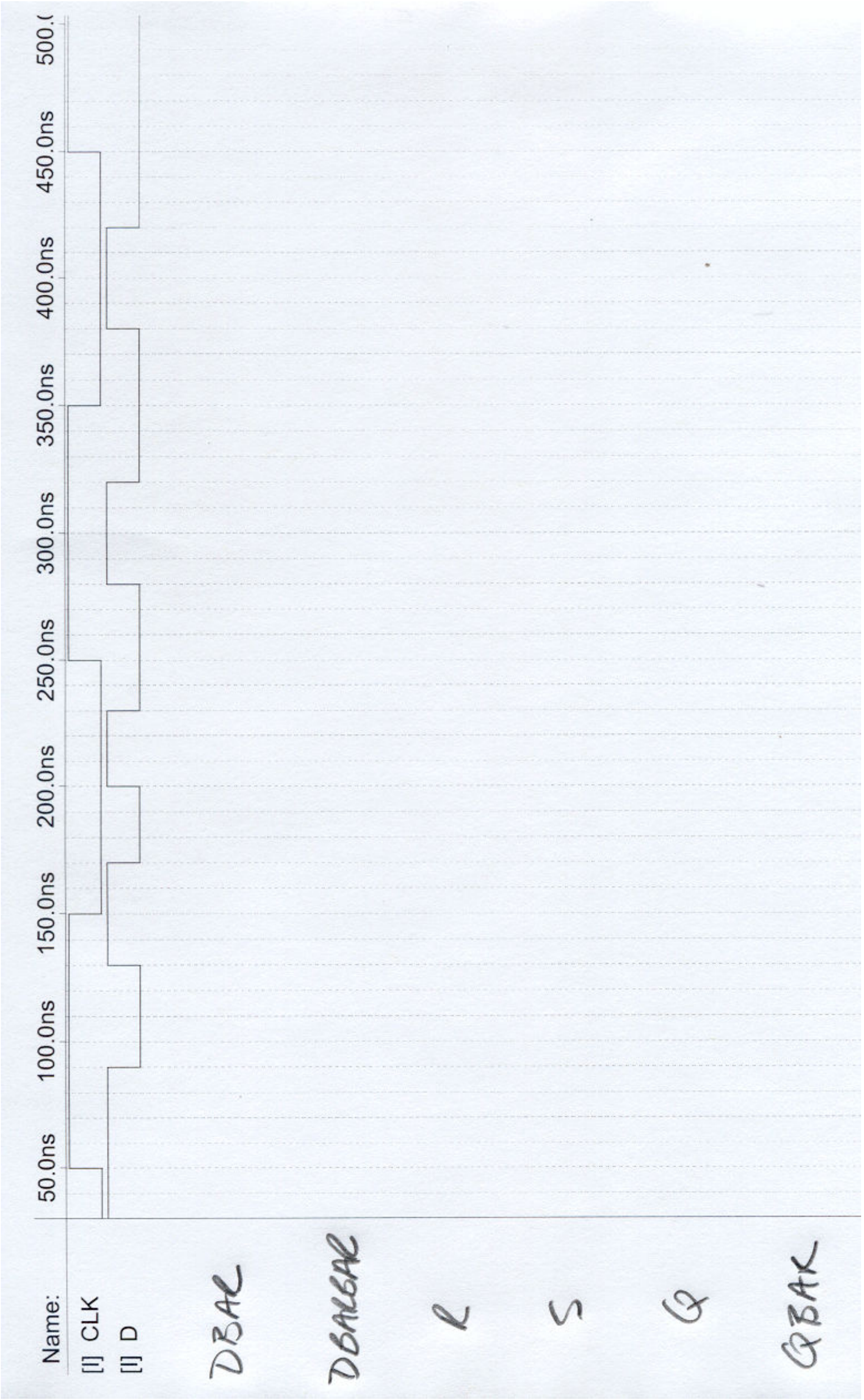
a) (26 points) For the edge-triggered D Flip-Flop shown below, complete the timing diagram on the following page. The actual propagation delays are not important, but use arrows to indicate the causality and order of transitions.

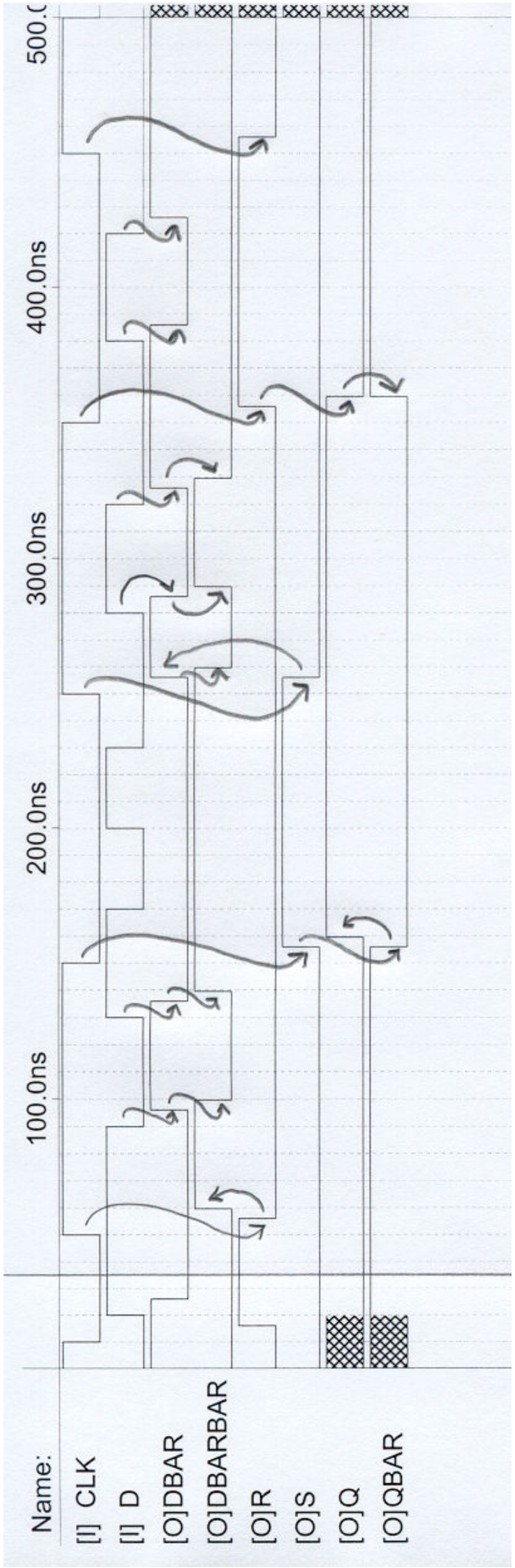
Assume the following initial conditions:

CLK = 0
D = 1

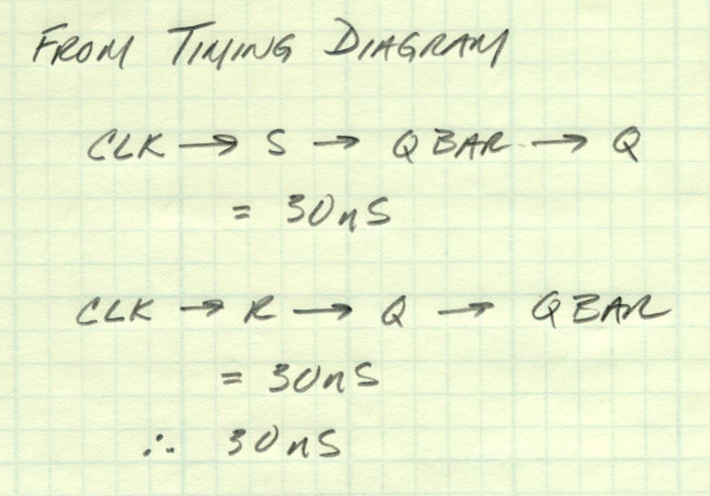
DBAR = 0
DBARBAR = 0
R = 1
S = 0
Q = 0
QBAR = 1




Name:
[I] CLK
[I] D
DBAR
DBARBAR
R
S
Q
QBAR
50.0ns
100.0ns
150.0ns
200.0ns
250.0ns
300.0ns
350.0ns
400.0ns
450.0ns
500.0


Name:
[I] CLK
[I] D
[O]DBAR
[O]DBARBAR
[O]R
[O]S
[O]Q
[O]QBAR
100.0ns
200.0ns
300.0ns
400.0ns
500.0

b) (3 points) Assuming that $t_{PHL} = t_{PLH} = 10\text{ns}$ for both the 2 and 3 input NOR gates, what is the worst case CLK to Q propagation delay?



FROM TIMING DIAGRAM

CLK → S → QBAR → Q

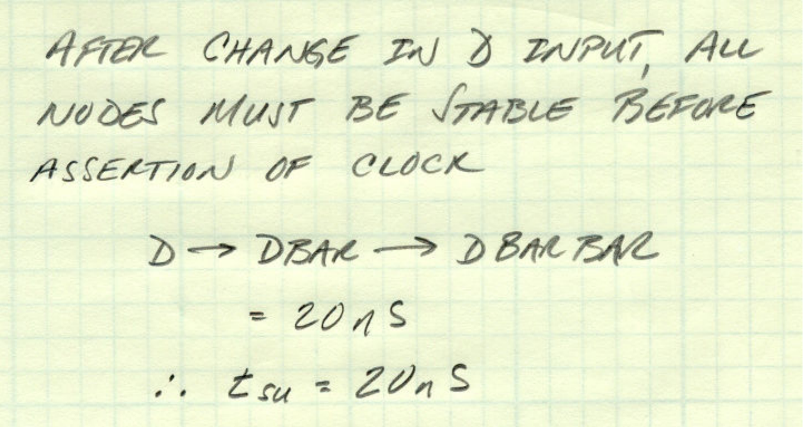
= 30nS

CLK → R → Q → QBAR

= 30nS

∴ 30nS

c) (3 points) If fundamental mode operation is assumed (and guaranteed) and the propagation delays are as specified in part b) above, what is the set up time for this flip flop?



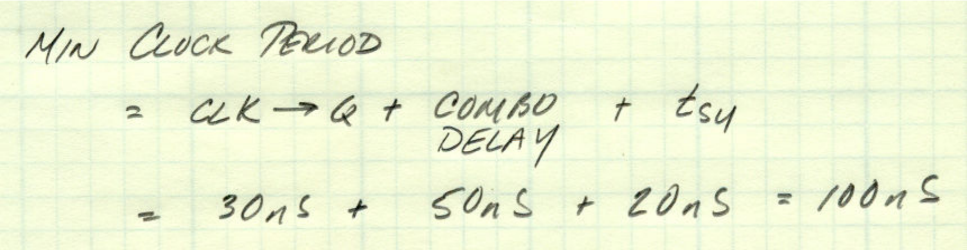
AFTER CHANGE IN D INPUT, ALL NODES MUST BE STABLE BEFORE ASSERTION OF CLOCK

D → DBAR → DBAR BAR

= 20nS

∴ t_{su} = 20nS

d) (3 points) If this flip flop is used in a digital system in conjunction with a combinational logic block having a critical path delay of 50ns, what is the minimum clock period for this system?



MIN CLOCK PERIOD

= CLK → Q + COMBO DELAY + t_{su}

= 30nS + 50nS + 20nS = 100nS

Problem #2.

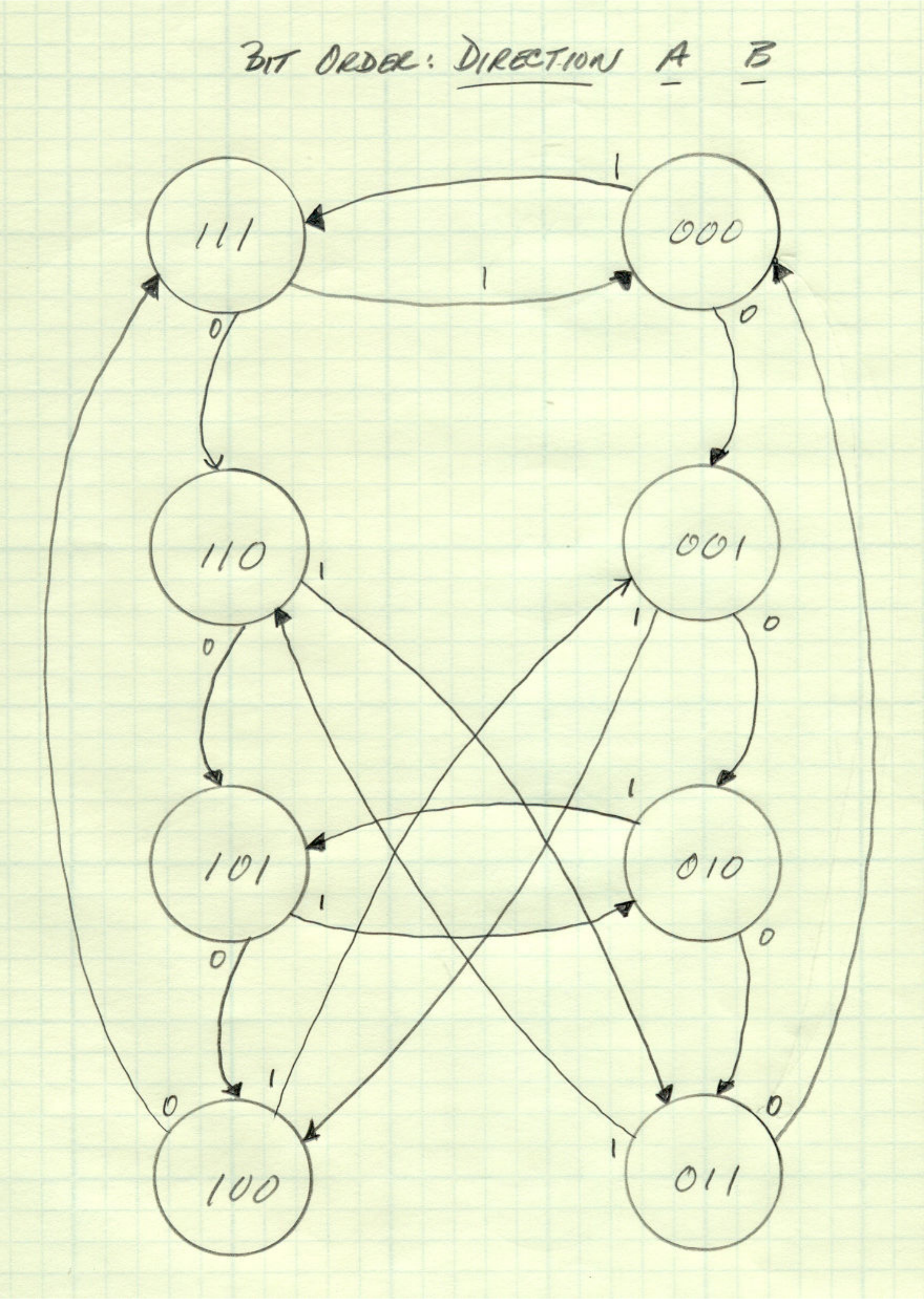
In this problem you are asked to design a 2-bit up/down binary counter. The counter has a single input R (Reverse). When R is 0, the counter continues counting in the current direction (up or down) on each clock edge. When R is 1, the direction is reversed i.e., if the counter had been counting up, it now counts down, if the counter had been counting down, it now begins counting up. Note that R doesn't *specify* the direction, it *reverses* the current direction.

The design may require more than two state variables, but the count must be represented by the two least significant state variables which must be labeled A and B (where B is the least significant bit).

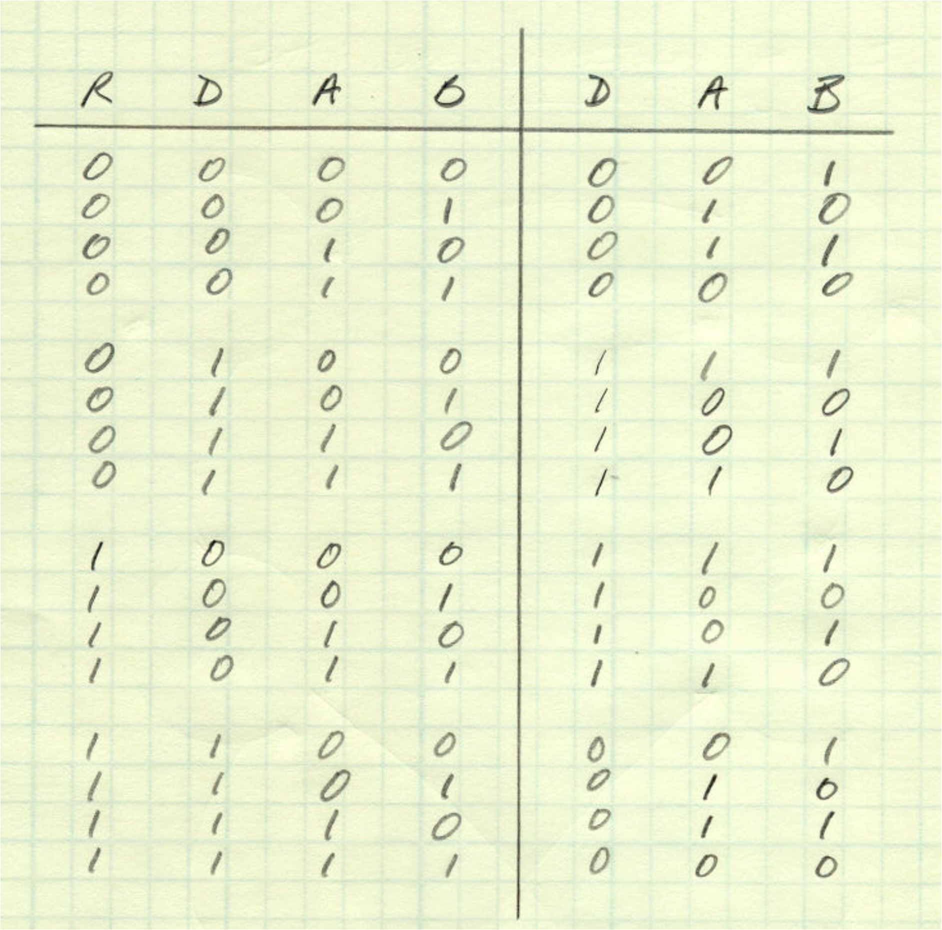
When counting up: AB = 00 → 01 → 10 → 11 → 00...
When counting down: AB = 11 → 10 → 01 → 00 → 11...

The count should change on every clock edge whether reversing direction or not.

a) (5 points) Construct a state diagram for your design. Clearly indicate the definition of each state variable in your design.

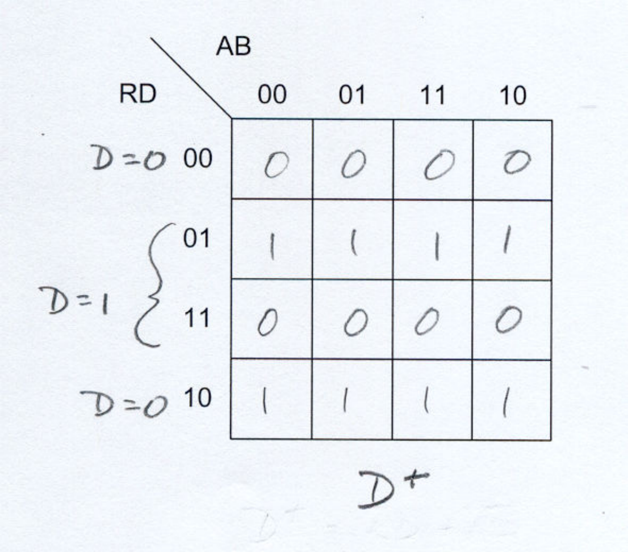


b) (10 points) Construct a state table for your design.



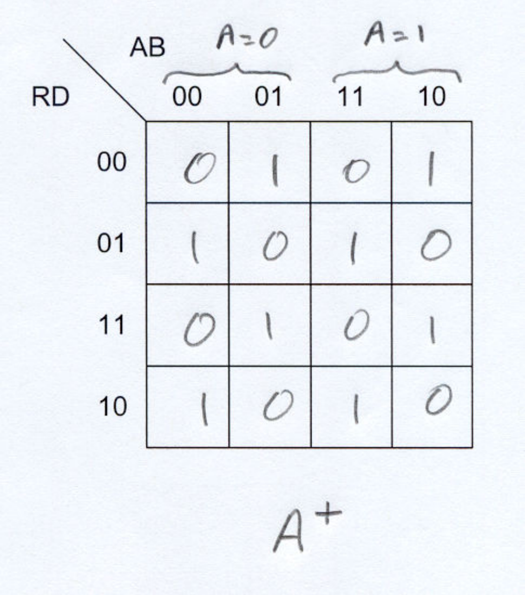
R	D	A	B	D	A	B
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	0	1	1	0	0	0
0	1	0	0	1	1	1
0	1	0	1	1	0	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	1	1	1
1	0	0	1	1	0	0
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	0	1	1
1	1	1	1	0	0	0

c) (5 points) Construct next state maps for each of the state variables in your design.



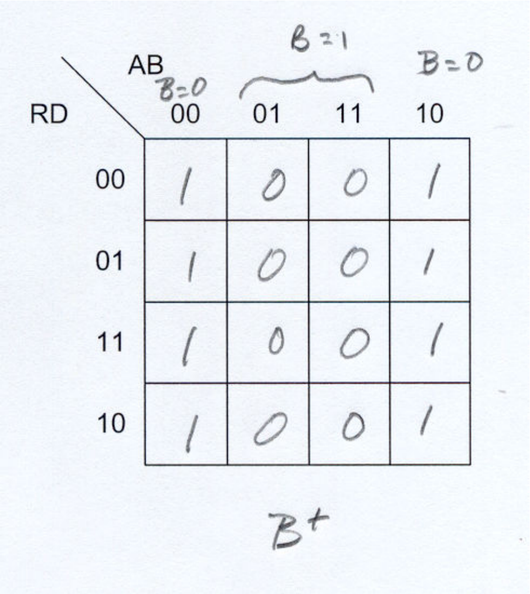
	AB RD	00	01	11	10
D=0	00	0	0	0	0
D=1	01	1	1	1	1
	11	0	0	0	0
D=0	10	1	1	1	1

D^+



AB	A=0		A=1	
RD	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

A^+

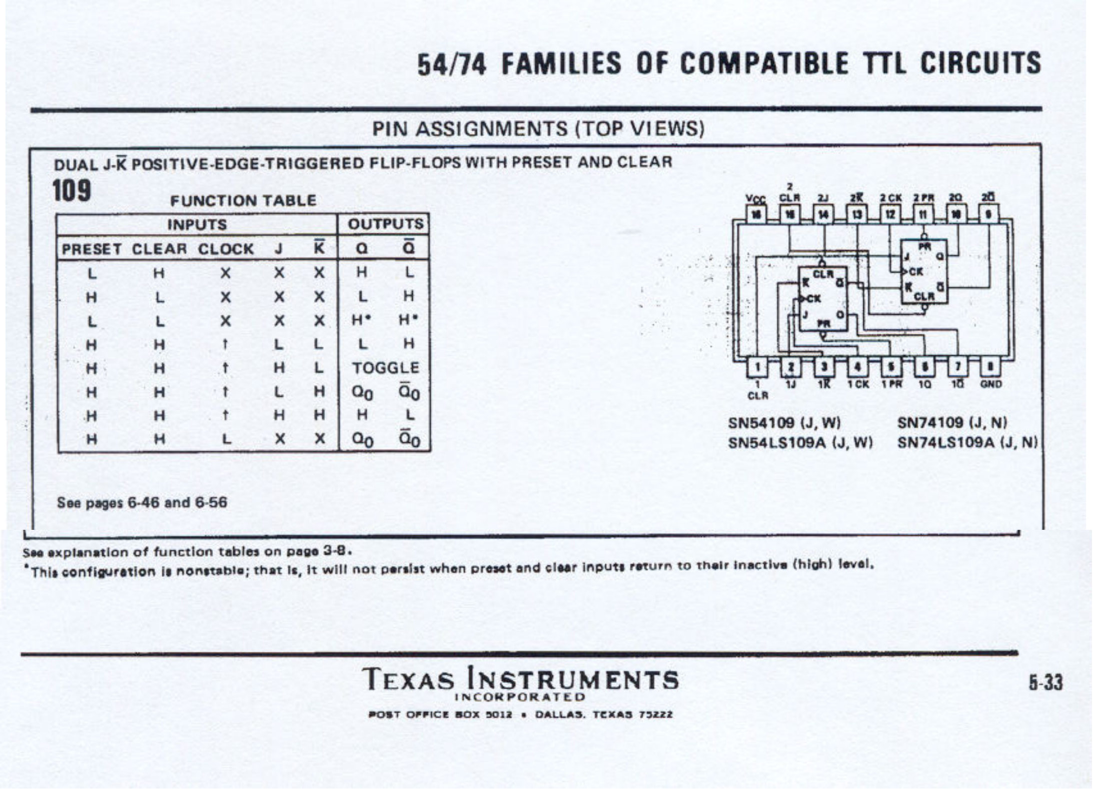


AB	B=0	B=1		B=0
RD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

B^+

d) (5 points) Marketing has determined that if 74109 “J – not K” flip flops are used, profit margins will be maximized. The pin assignments and function table for the device are given below.

Construct the excitation table for the “J – not K” flip flop.



54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

VCC
2 CLR
2J
2$\overline{K}$
2 CK
2 PR
2Q
2$\overline{Q}$
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
1 CLR
1J
1$\overline{K}$
1 CK
1 PR
1Q
1$\overline{Q}$
GND
CLR
PR
J
CK
K
Q
$\overline{Q}$

SN54109 (J, W) SN74109 (J, N)
SN54LS109A (J, W) SN74LS109A (J, N)

See pages 6-46 and 6-56

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

TEXAS INSTRUMENTS
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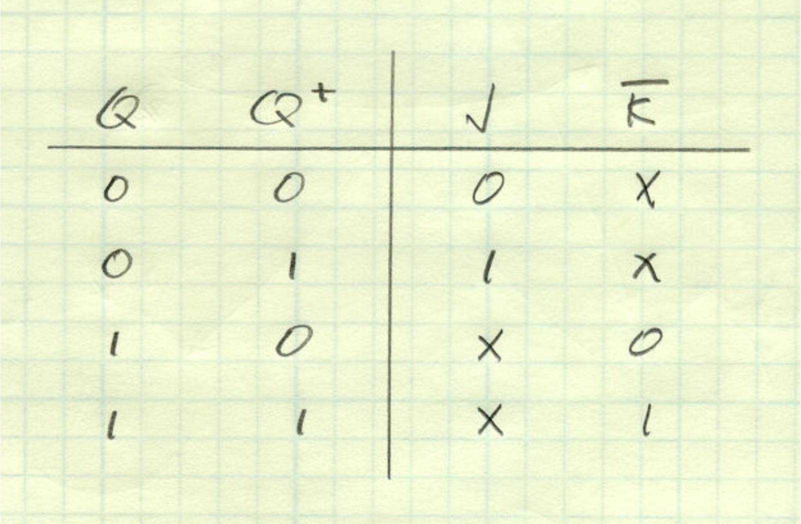


Q	Q^+	J	$\overline{K}$
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

e) (10 points) Based on the excitation table derived in part d) above, determine the flip flop inputs for each of the state variables. You can assume that the preset and clear inputs are always tied to a logical 1.

RD \ AB	00	01	11	10
00	0	0	0	0
01	X	X	X	X
11	X	X	X	X
10	1	1	1	1

$J_D = R$

RD \ AB	00	01	11	10
00	X	X	X	X
01	1	1	1	1
11	0	0	0	0
10	X	X	X	X

$\overline{K}_D = \overline{R}$

RD \ AB	00	01	11	10
00	0	1	X	X
01	1	0	X	X
11	0	1	X	X
10	1	0	X	X

$$J_A = \bar{R}\bar{D}B + \bar{R}D\bar{B} + RDB + R\bar{D}\bar{B}$$
$$= R \oplus D \oplus B$$

RD \ AB	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

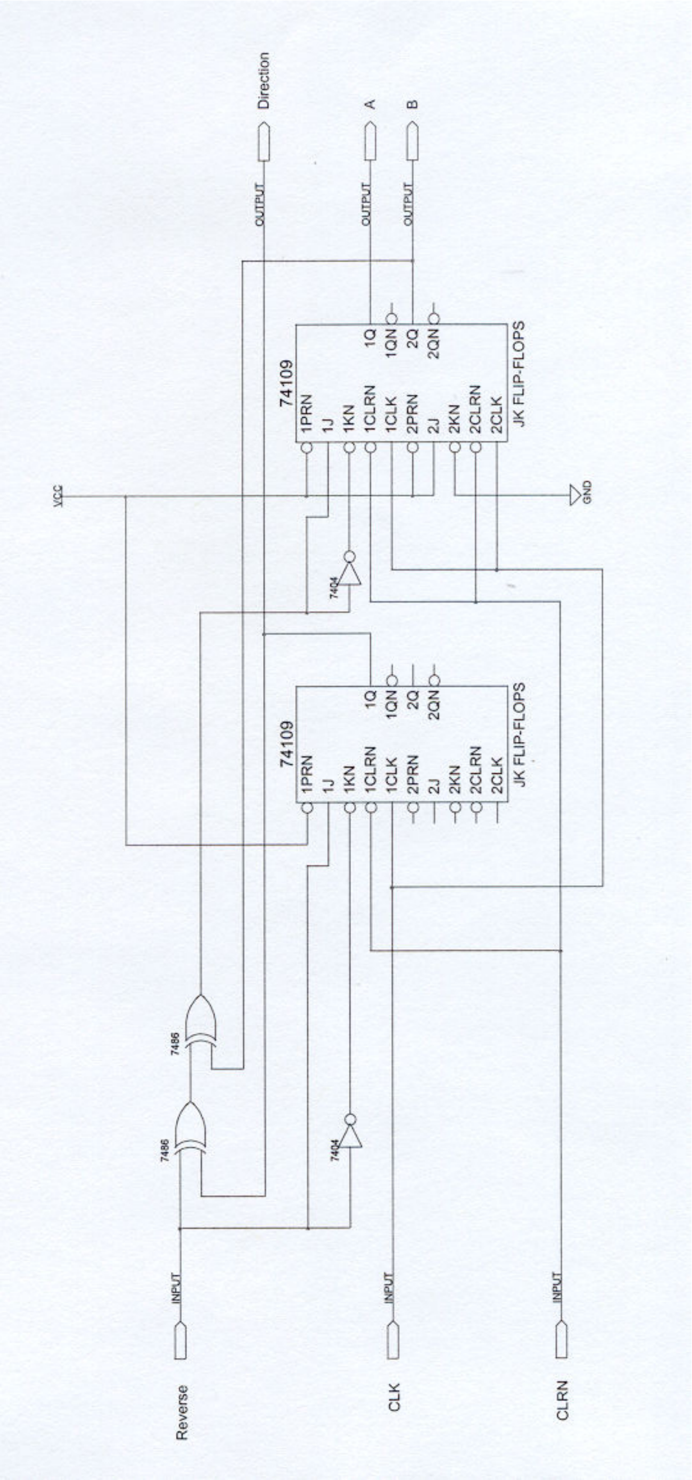
$$J_B = 1$$

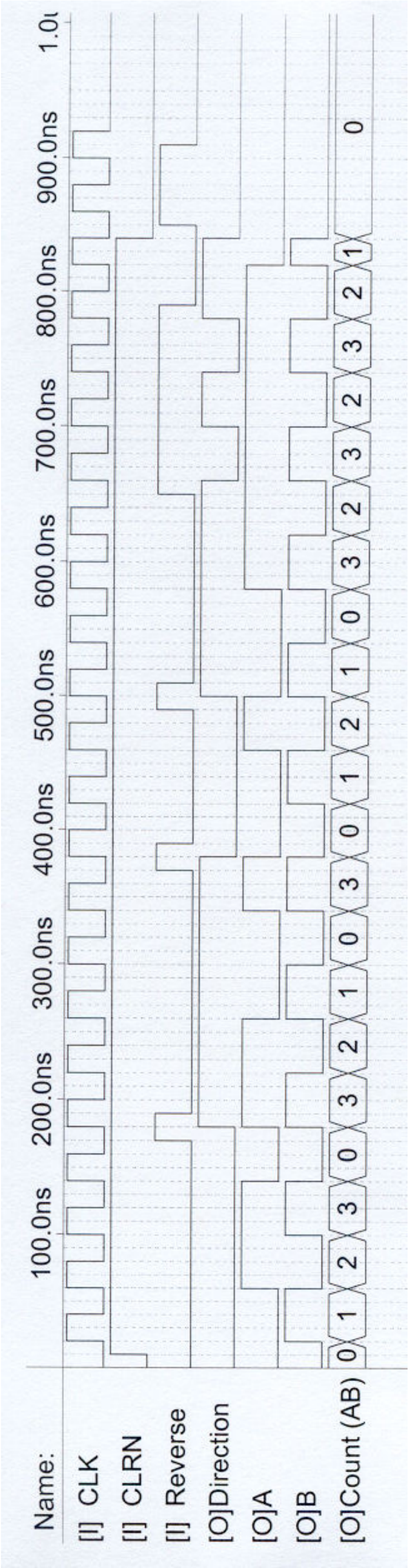
RD \ AB	00	01	11	10
00	X	X	0	1
01	X	X	1	0
11	X	X	0	1
10	X	X	1	0

$$K_A = \bar{R}\bar{D}\bar{B} + \bar{R}DB + RD\bar{B} + R\bar{D}B$$
$$= (R \oplus D \oplus B)'$$

RD \ AB	00	01	11	10
00	X	0	0	X
01	X	0	0	X
11	X	0	0	X
10	X	0	0	X

$$K_B = 0$$


VCC
GND
74109
1PRN
1J
1KN
1CLRN
1CLK
2PRN
2J
2KN
2CLRN
2CLK
1Q
1QN
2Q
2QN
JK FLIP-FLOPS
74109
JK FLIP-FLOPS
7404
7404
7486
7486
INPUT
INPUT
INPUT
OUTPUT
OUTPUT
OUTPUT
Reverse
CLK
CLRN
Direction
A
B


Name:
[I] CLK
[I] CLRN
[I] Reverse
[O]Direction
[O]A
[O]B
[O]Count (AB)
100.0ns
200.0ns
300.0ns
400.0ns
500.0ns
600.0ns
700.0ns
800.0ns
900.0ns
1.0u
0
1
2
3
0
3
2
1
0
3
0
1
2
1
0
3
2
3
2
3
2
1
0

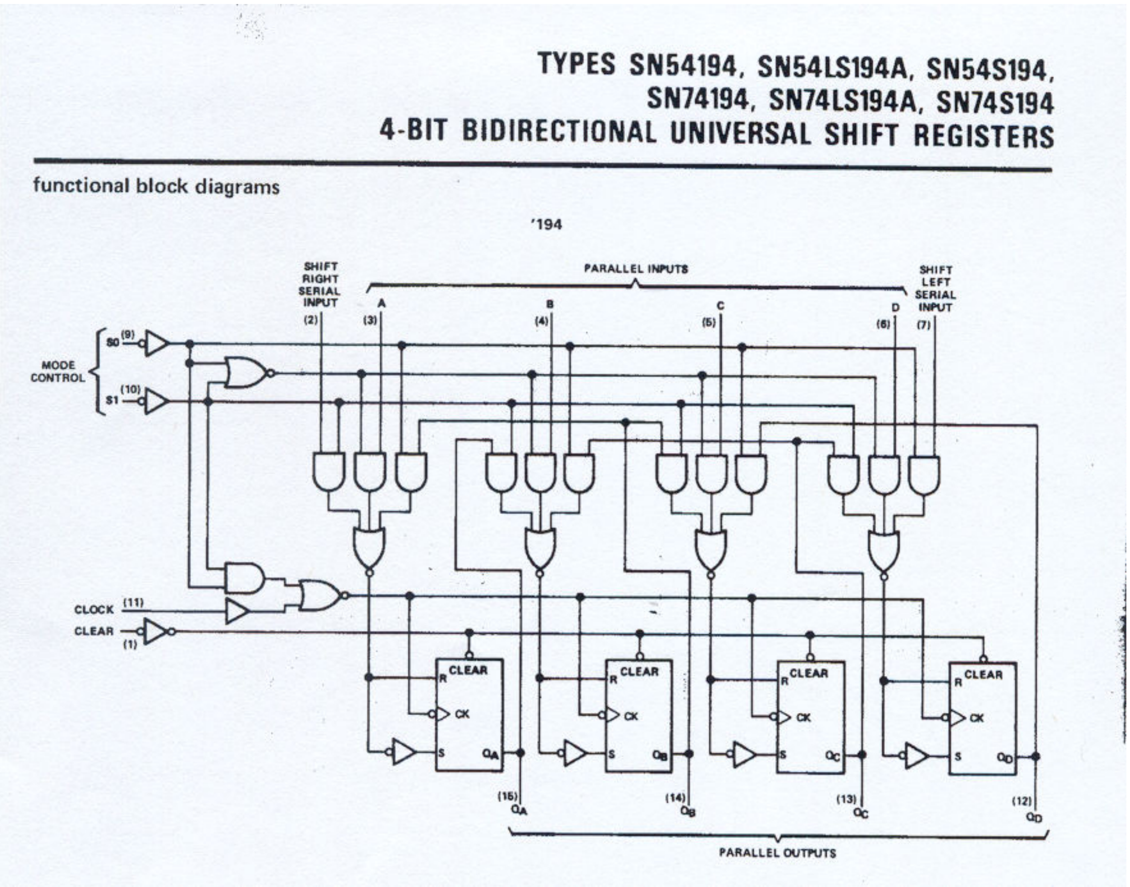
Problem #3.

On this and the following two pages are the functional block diagram, data sheet and timing diagram, respectively, for the SN74194 4-Bit Bidirectional Universal Shift Register.

The Function Table on the data sheet on the following page provides all the information necessary to complete this design, but I've included all three pages from "*The TTL Data Book for Design Engineers*" so that there will be no ambiguity as to how this device operates.

On the final pages of this exam, give the Verilog code that, when synthesized, will implement the SN74194 on an FPGA. Use the signal names given in the module declaration in your design.

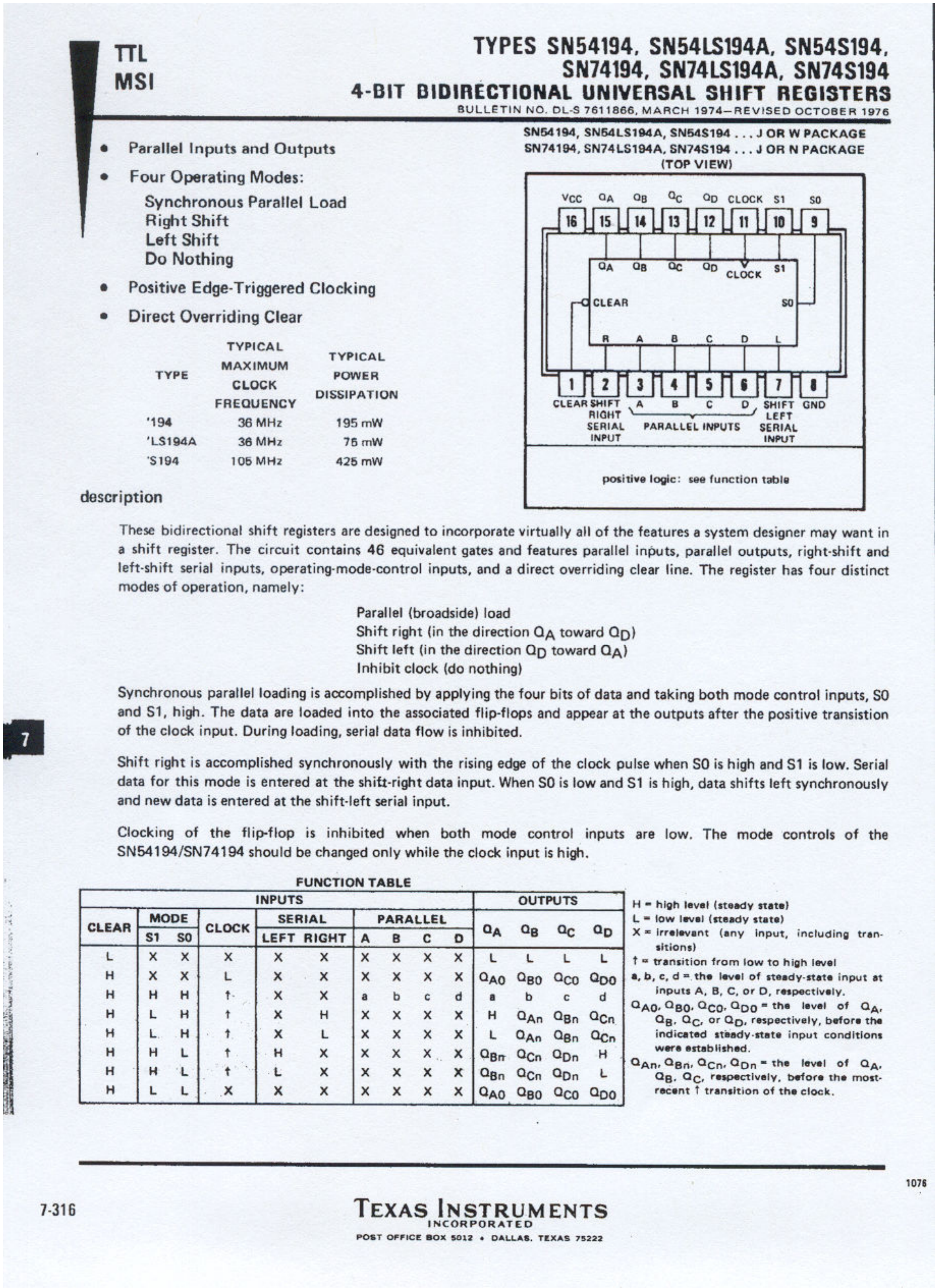
The syntax of your design will be checked very carefully to determine if it meets the specification.



TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

functional block diagrams

'194



TTL
MSI

TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7611866, MARCH 1974—REVISED OCTOBER 1976

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 . . . J OR N PACKAGE
(TOP VIEW)

positive logic: see function table

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

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FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

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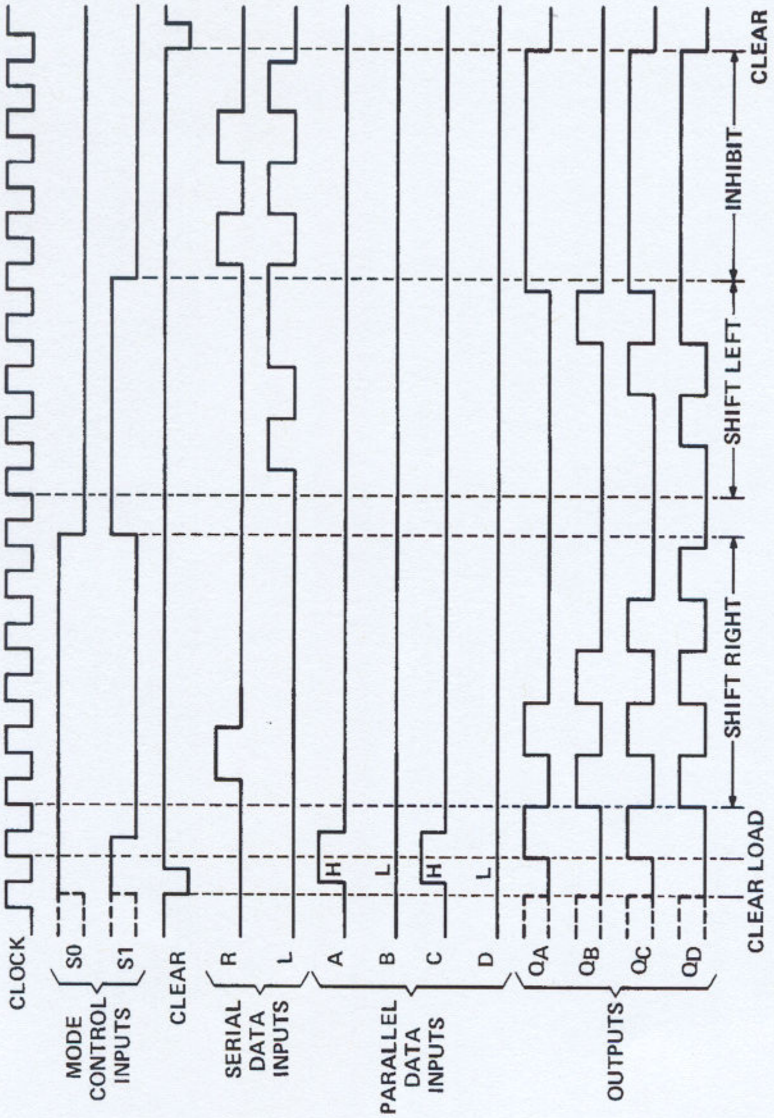
TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



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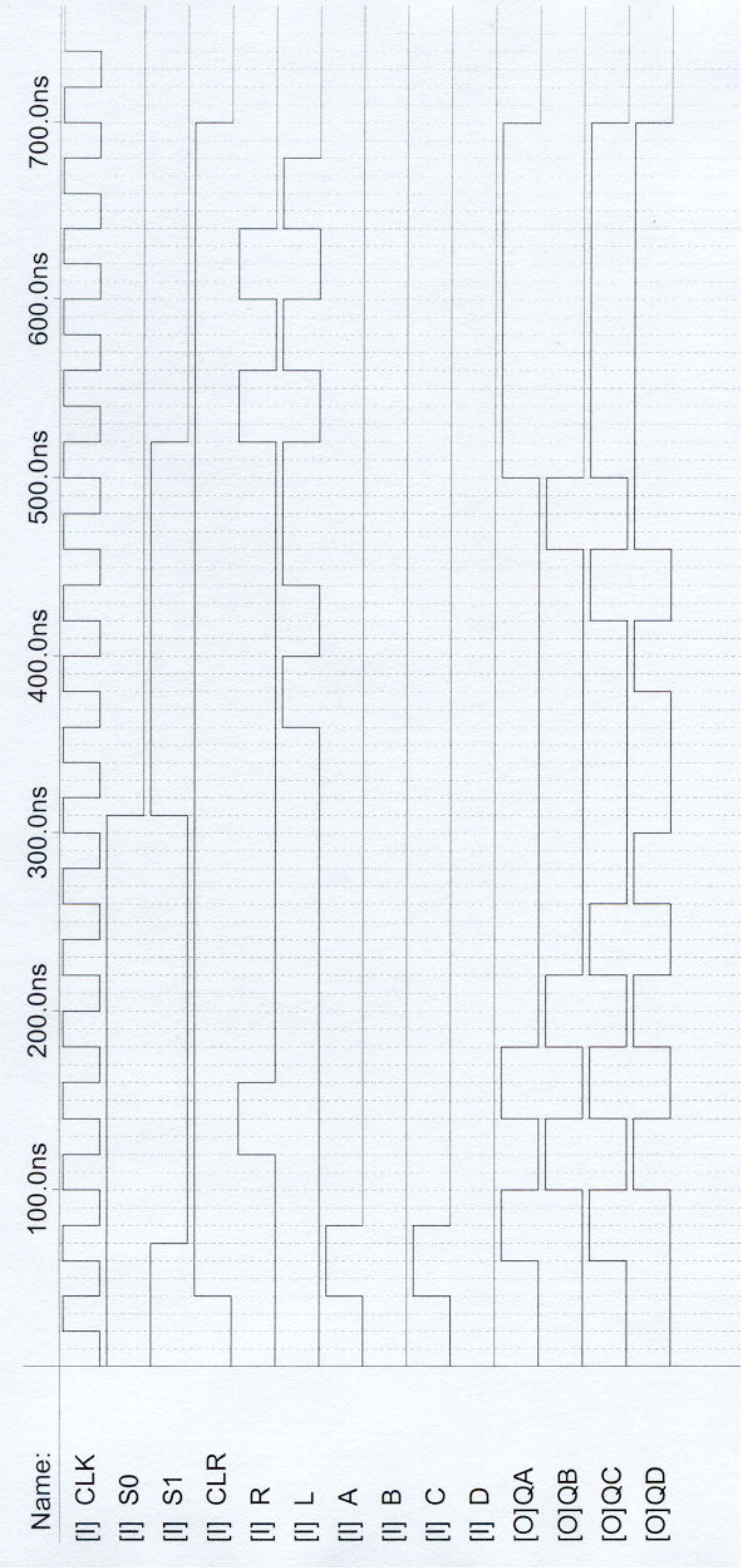
// module SN74194 (QA, QB, QC, QD, CLR, S1, S0, CLK, L, R, A, B, C, D);

// (6 points for structure and “always” syntax; 6 points per operation)

```
module SN74194 (QA, QB, QC, QD, CLR, S1, S0, CLK, L, R, A, B, C, D);

output QA, QB, QC, QD;
input CLR, S1, S0, CLK, L, R, A, B, C, D;

reg QA, QB, QC, QD;

always @ (posedge CLK or negedge CLR)      // this must be negedge CLR,
                                           // not just CLR...

if (!CLR)           // CLR is the highest priority, so it must
begin               // be tested first...it overrides the values
  QA <= 0;          // of S1 and S0
  QB <= 0;
  QC <= 0;
  QD <= 0;
end

else if (S1 && S0)
begin
  QA <= A;          // S1 == S0 == 1
  QB <= B;          // is the parallel load
  QC <= C;          // operation
  QD <= D;
end

else if (!S1 && S0)      // shift right (toward QD)
begin
  QA <= R;
  QB <= QA;         // if blocking assignments are used
  QC <= QB;         // the order must be reversed, otherwise
  QD <= QC;         // R would be loaded into all registers
end

else if (S1 && !S0)      // shift left (toward QA)
begin
  QA <= QB;         // this order would actually
  QB <= QC;         // work for either blocking
  QC <= QD;         // of non-blocking assignments
  QD <= L;
end

                         // you could include a test for S1 == S0 == 0
                         // or a default else, but since the action is
                         // to do nothing, it's not necessary

endmodule
```

// endmodule


Name:
[I] CLK
[I] S0
[I] S1
[I] CLR
[I] R
[I] L
[I] A
[I] B
[I] C
[I] D
[O]QA
[O]QB
[O]QC
[O]QD
100.0ns
200.0ns
300.0ns
400.0ns
500.0ns
600.0ns
700.0ns